COLORADO STATE UNIVERSITY

Life-after-Death: Exploring Thermal Annealing Conditions to Enhance 3D NAND SSD Endurance

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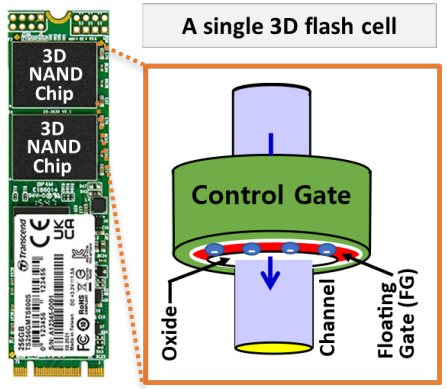
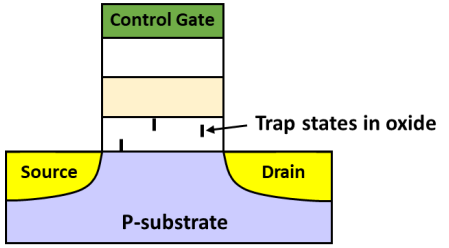
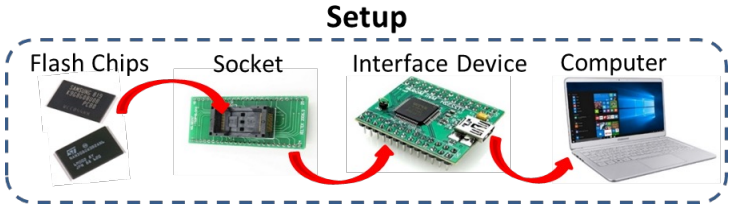
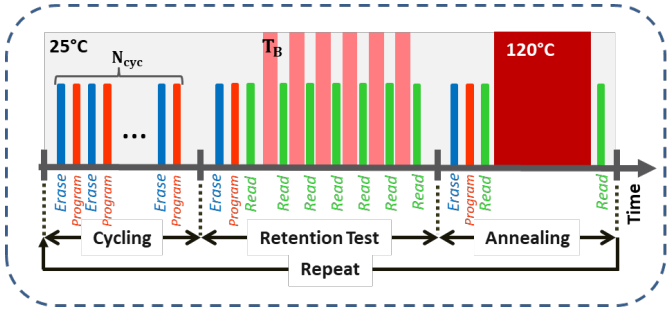
Outline

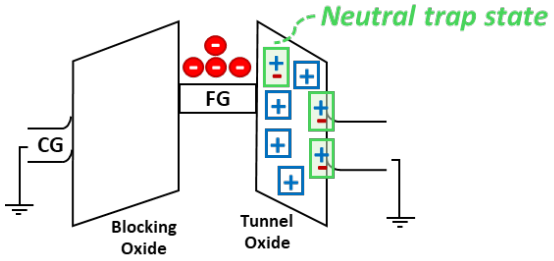
- Motivation and Background
- Experimental Setup and Samples
- Experimental Flow
- Results and Discussion
- Physics Explanation
- Conclusion

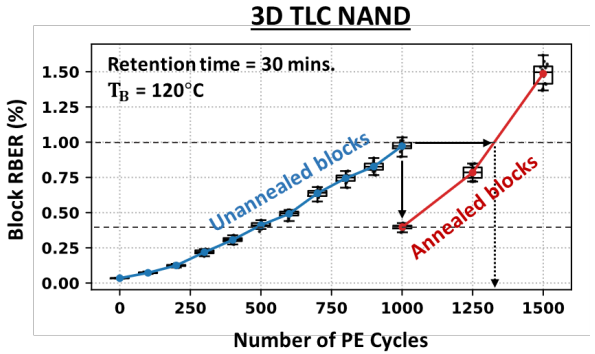




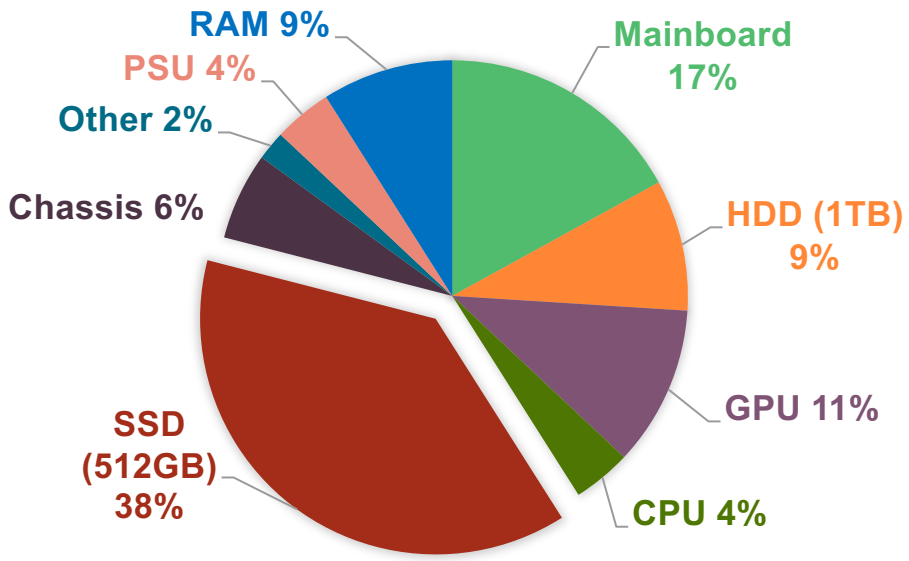








Motivation



Share of global warming potential by component (raw material), data derived from [Tannu 2023]

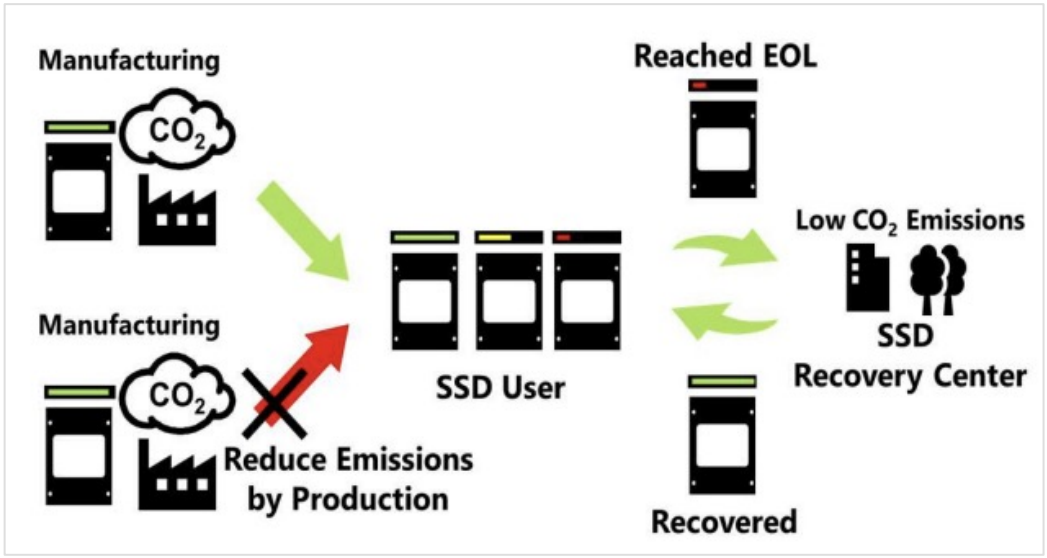
Tannu, Swamit, and Prashant J. Nair. "The dirty secret of ssds: Embodied carbon." ACM SIGENERGY Energy Informatics Review 3.3 (2023): 4-9.

SSDs Are Worse for the Planet Than HDDs: Report

News By Francisco Pires published August 10, 2022

HDDs get another green ally in their fight against their younger, faster siblings.

Comments (37)



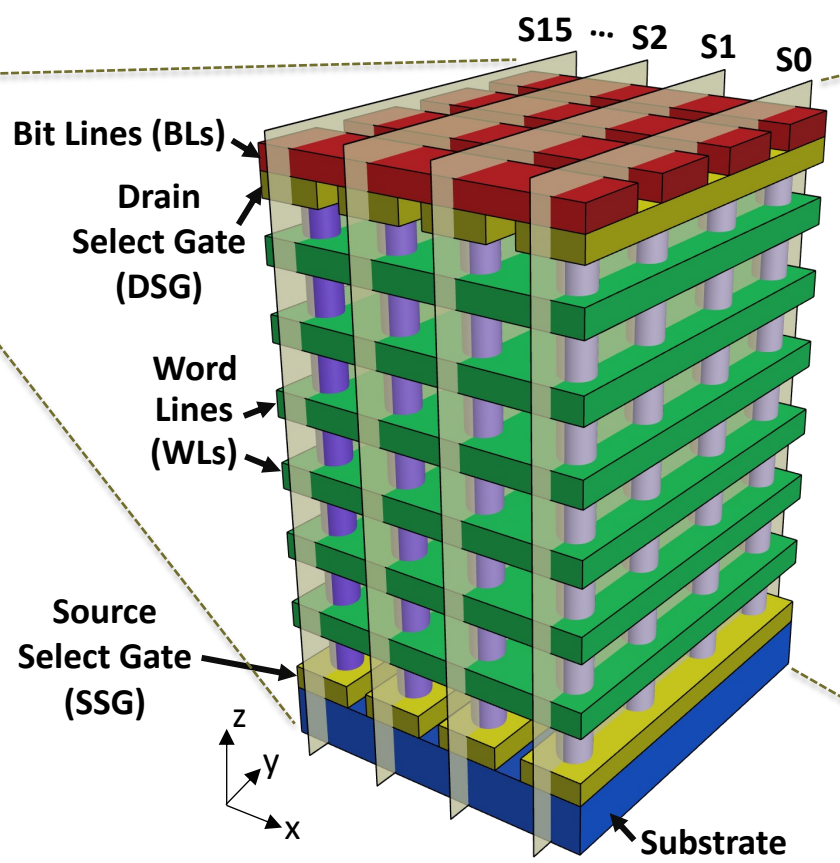
H. Tanaka et al., "Overcome the End of Life of 3D Flash Memory by Recovery Annealing, Aiming for Carbon Neutrality in Semiconductor Manufacturing," 2024 IEEE International Memory Workshop (IMW), Seoul, Korea, Republic of, 2024, pp. 1-4.

SSD production has generated much more carbon dioxide compared to Hard Disk Drive (HDD).
Reusing SSDs can help reduce carbon footprint.

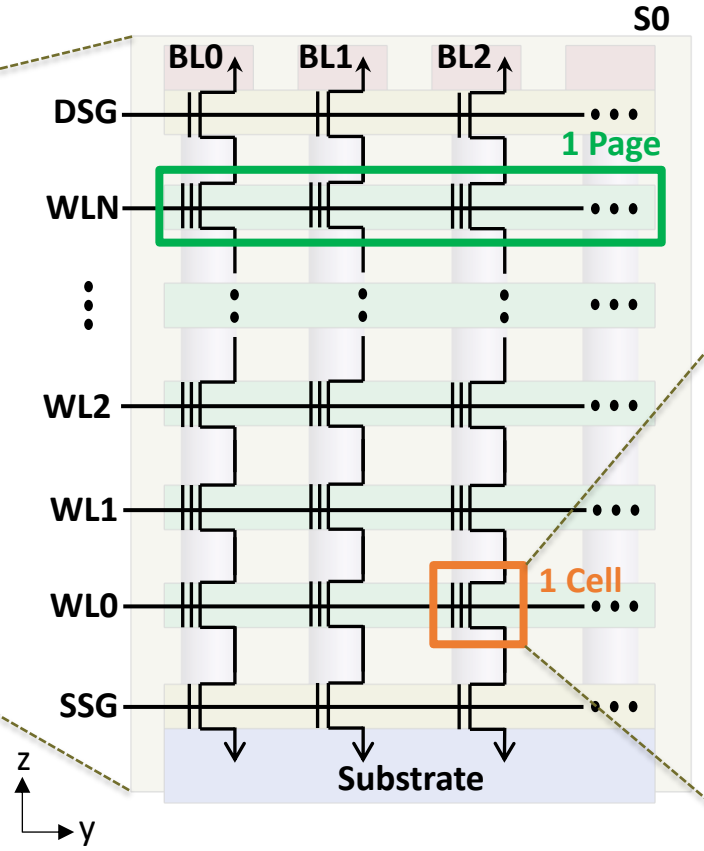
Background: NAND flash-based SSD

Flash-based SSD

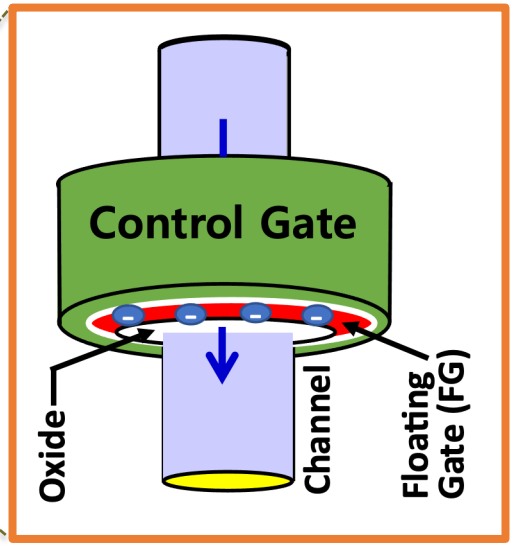
Schematic of a 3D flash block



Circuit diagram of physical sub-block

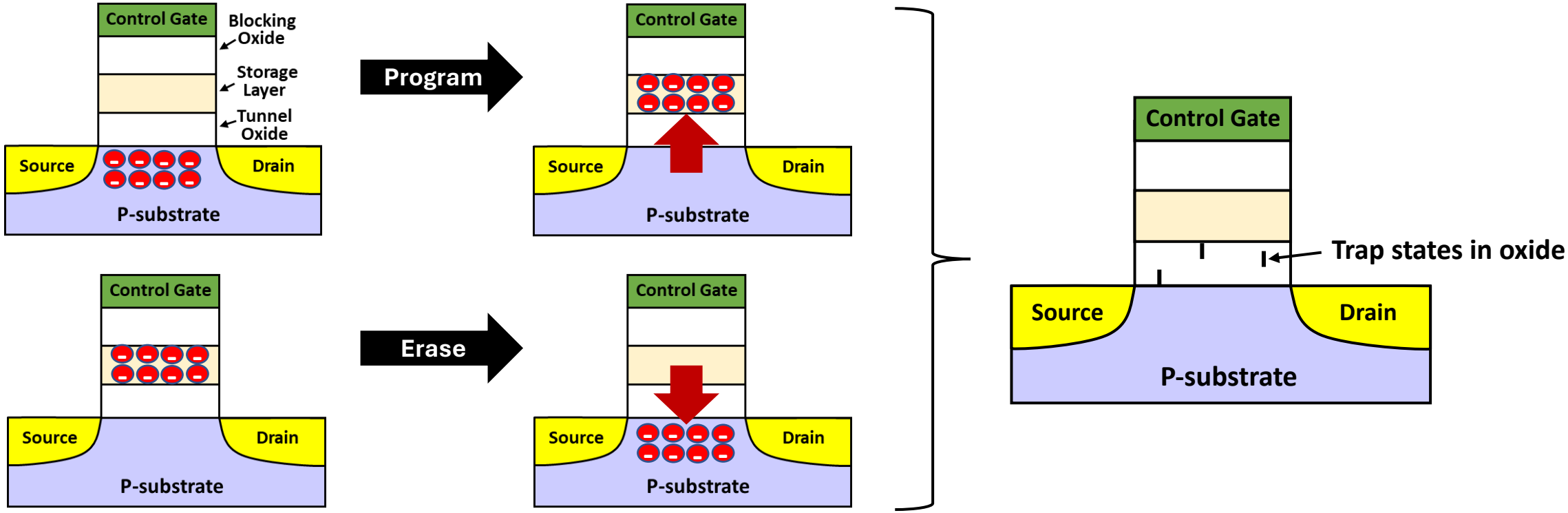


A single 3D flash cell



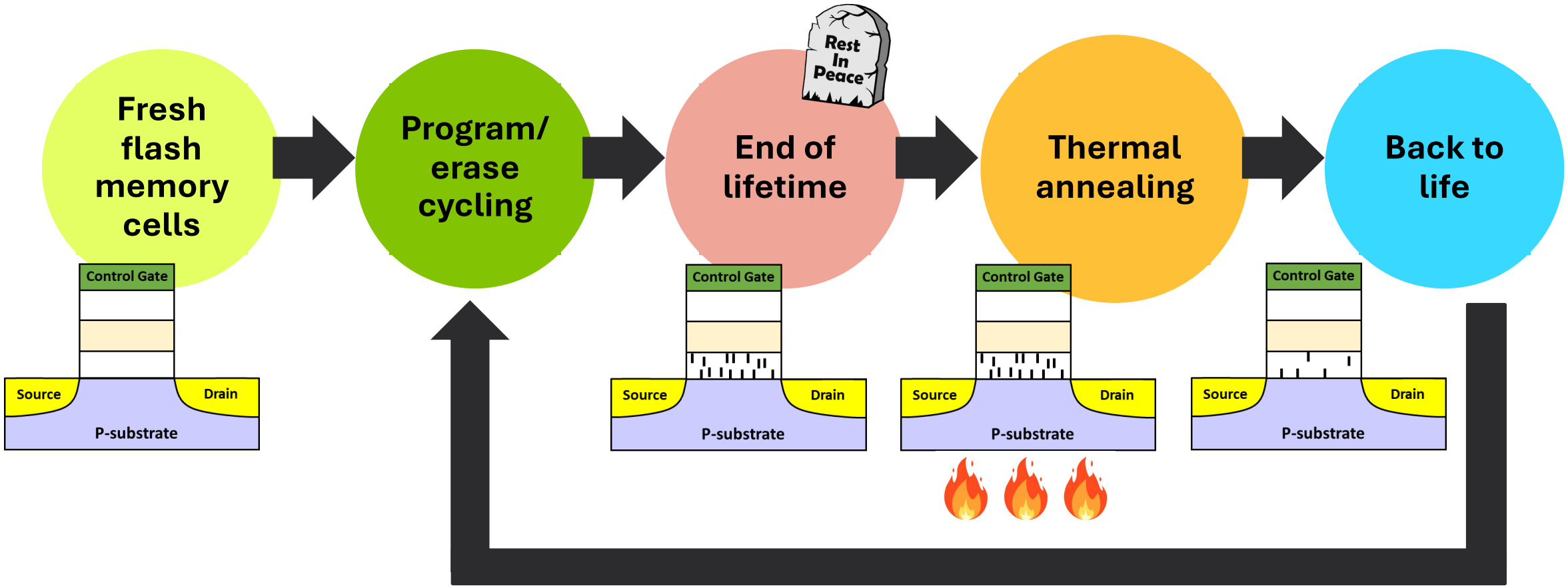
A single NAND flash chip contains million of flash cells and each cell can store user's information.

Background: Program vs. Erase Flash Cell



Electrons move through the tunnel oxide layer during P/E cycling, resulting in damage in the oxide layer.
The damage comes in the form of trap states.

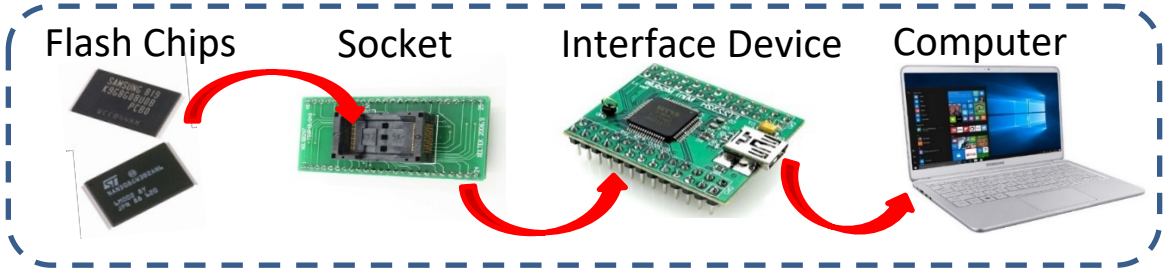
Life-after-Death After Thermal Annealing



Thermal annealing can alleviate damage in the oxide layer, as a result, the worn-out flash cells can be reused again.

Experimental Setup and Samples

Setup

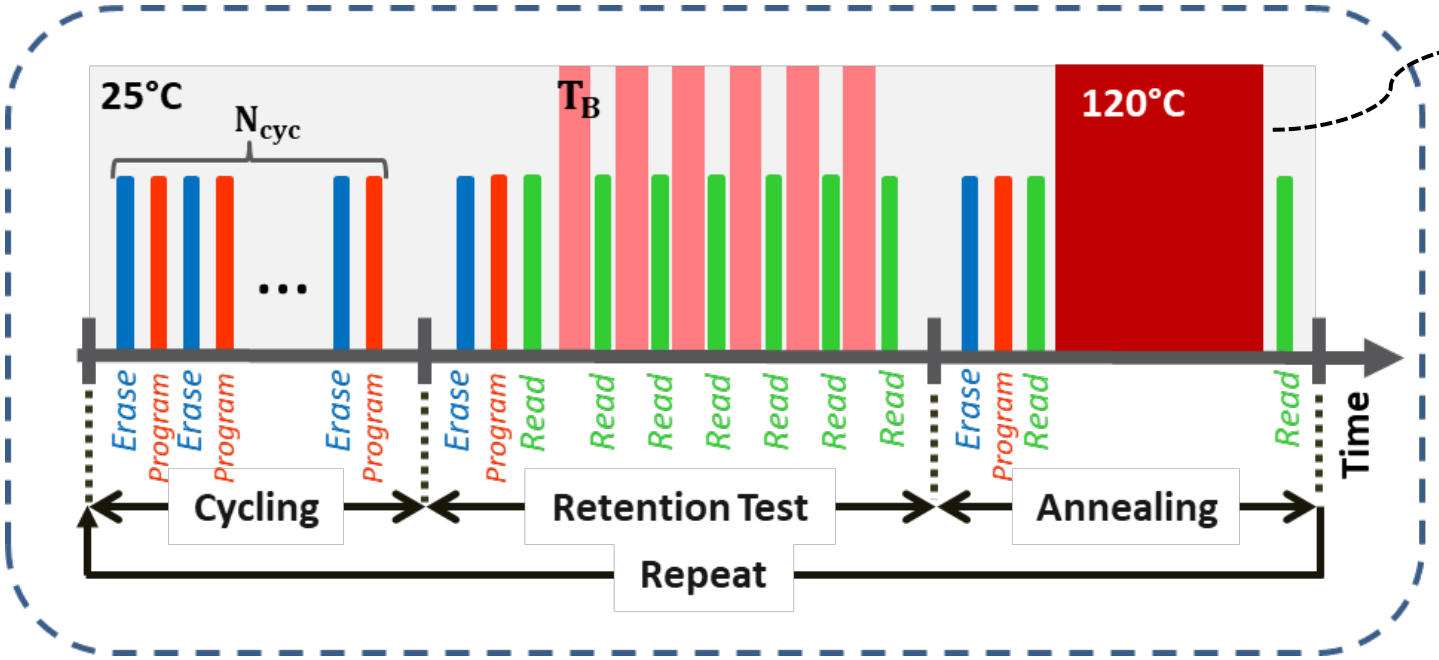


Samples

Sample	Details	Block size	Page size	Bytes per page	Endurance (PE cycles)
3D FG TLC	256GB 64 layers	1,008	2,304	16,384	1,000
3D FG MLC	256GB 32 layers	2,192	1,024	16,384	3,500

We used a custom hardware board to interface with commercial-off-the-shelf (COTS) memory chips.
Both 3D TLC and 3D MLC NAND flash memory chips are used in this work.

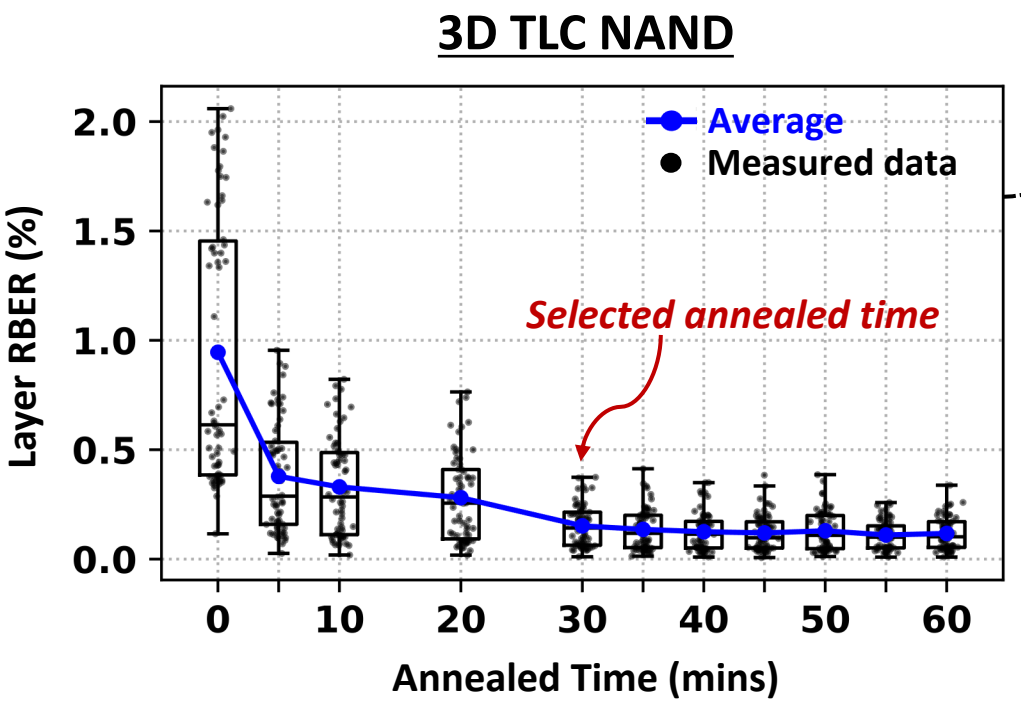
Experimental Flow



Aim to optimize annealing effects	
1) annealing temperature	120°C
2) annealing time	?
3) state of memory cells	?

Our experimental flow can break into three different parts – cycling, retention test, and thermal annealing. T_B is baking temperature and it can be at room temperature. However, we bake the chips at high temperature to accelerate data retention loss.

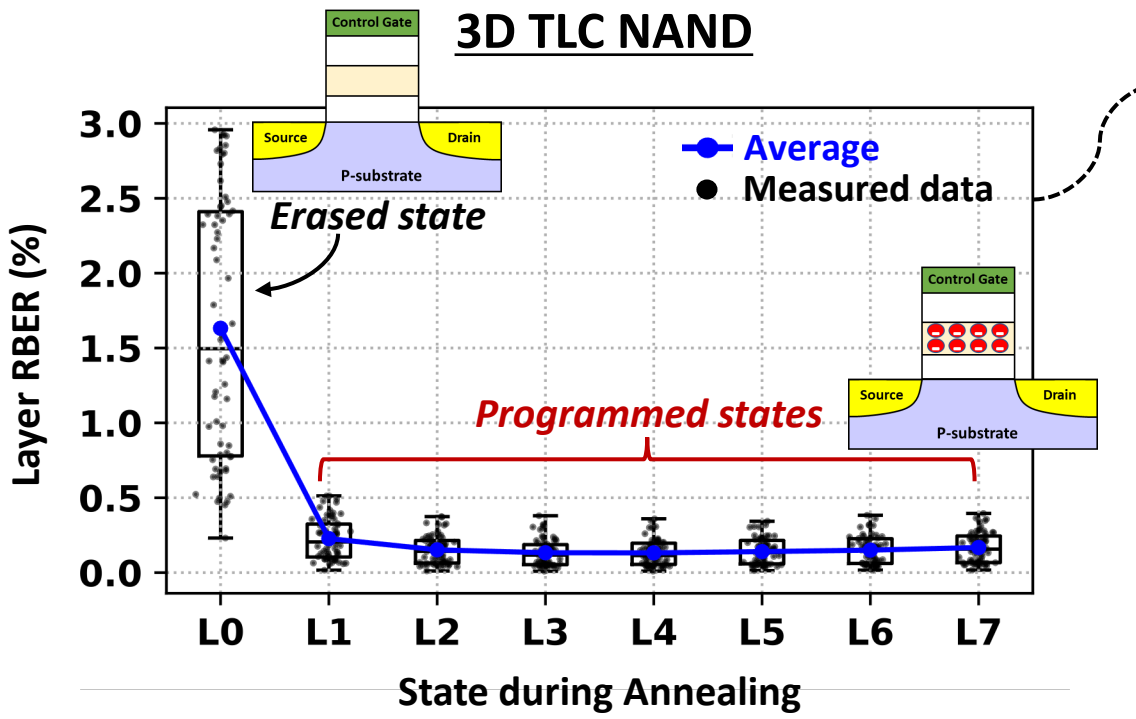
Evaluating Optimal Annealed Time



Aim to optimize annealing effects	
1) annealing temperature	120°C
2) annealing time	30 minutes
3) state of memory cells	?

Annealing based-improvement is saturated after 30 minutes of thermal annealing at 120°C.

Evaluating the Impact of State of Memory during Annealing

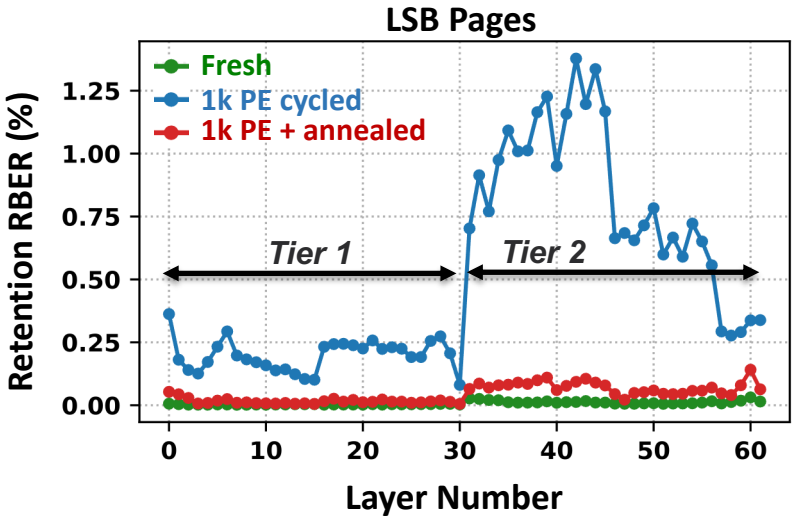


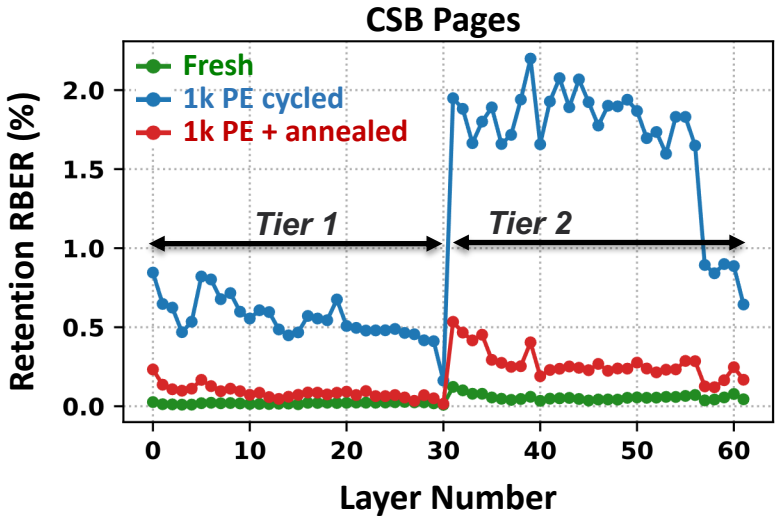
Aim to optimize annealing effects	
1) annealing temperature	120°C
2) annealing time	30 minutes
3) state of memory cells	Programmed state

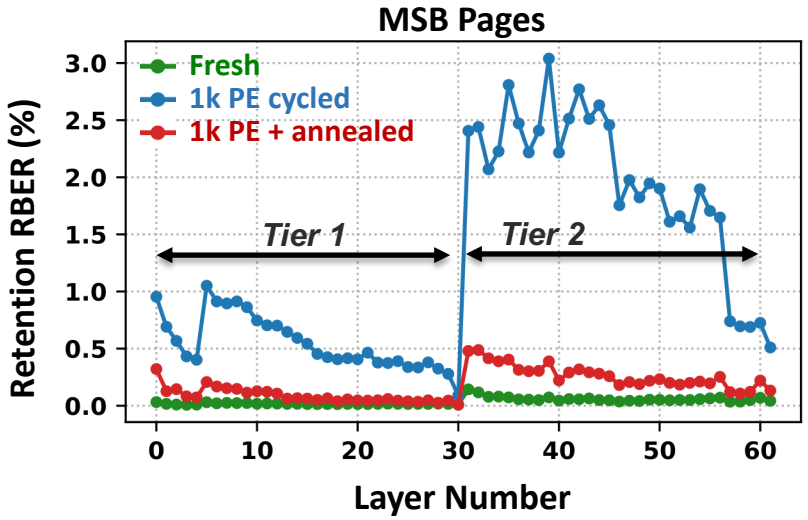
Leaving the memory cells in programmed states during the thermal annealing gives the smallest retention RBER through time compared to the erased state cell.

Results: Effects on Vertical Layers

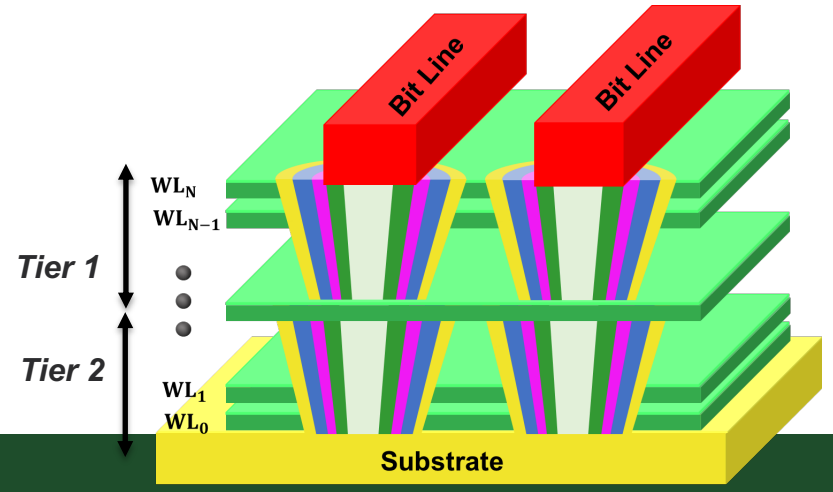
3D TLC NAND





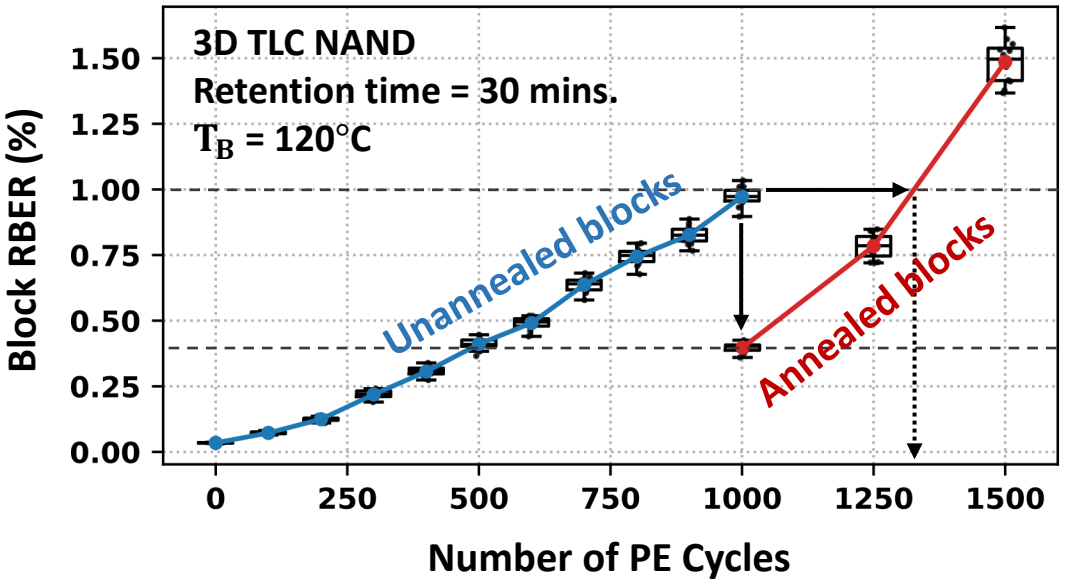


Annealing has a substantial impact on improving the RBER of the worn-out memory block. The post-annealing RBER (red line) of the LSB pages becomes closely comparable to the RBER of the fresh memory condition (green line).

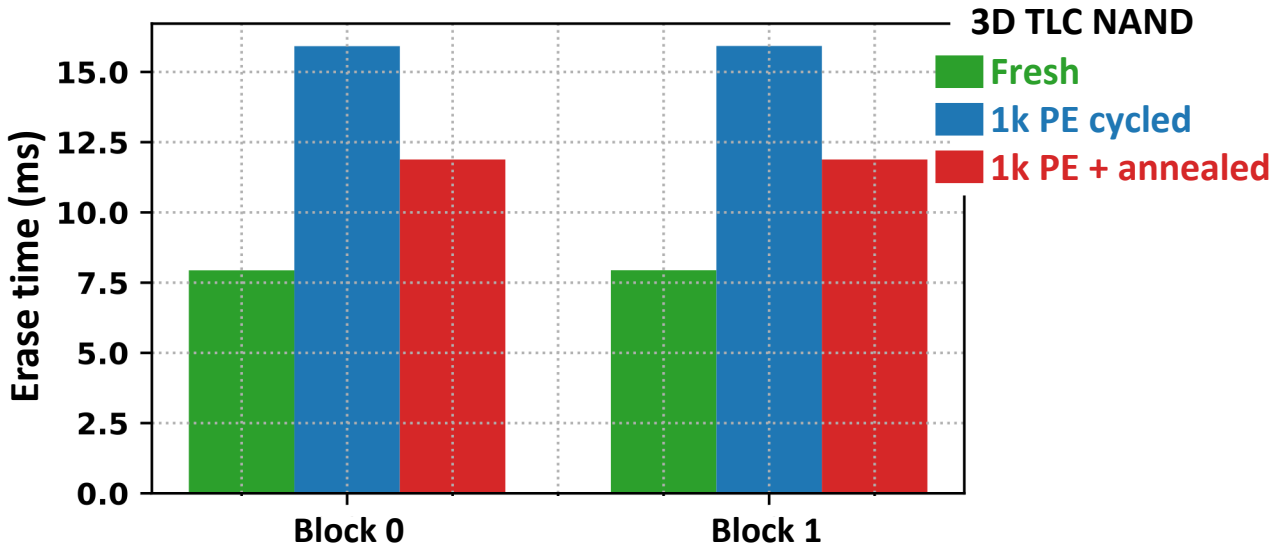


Results: Endurance and Erase Time Improvement

Block RBER

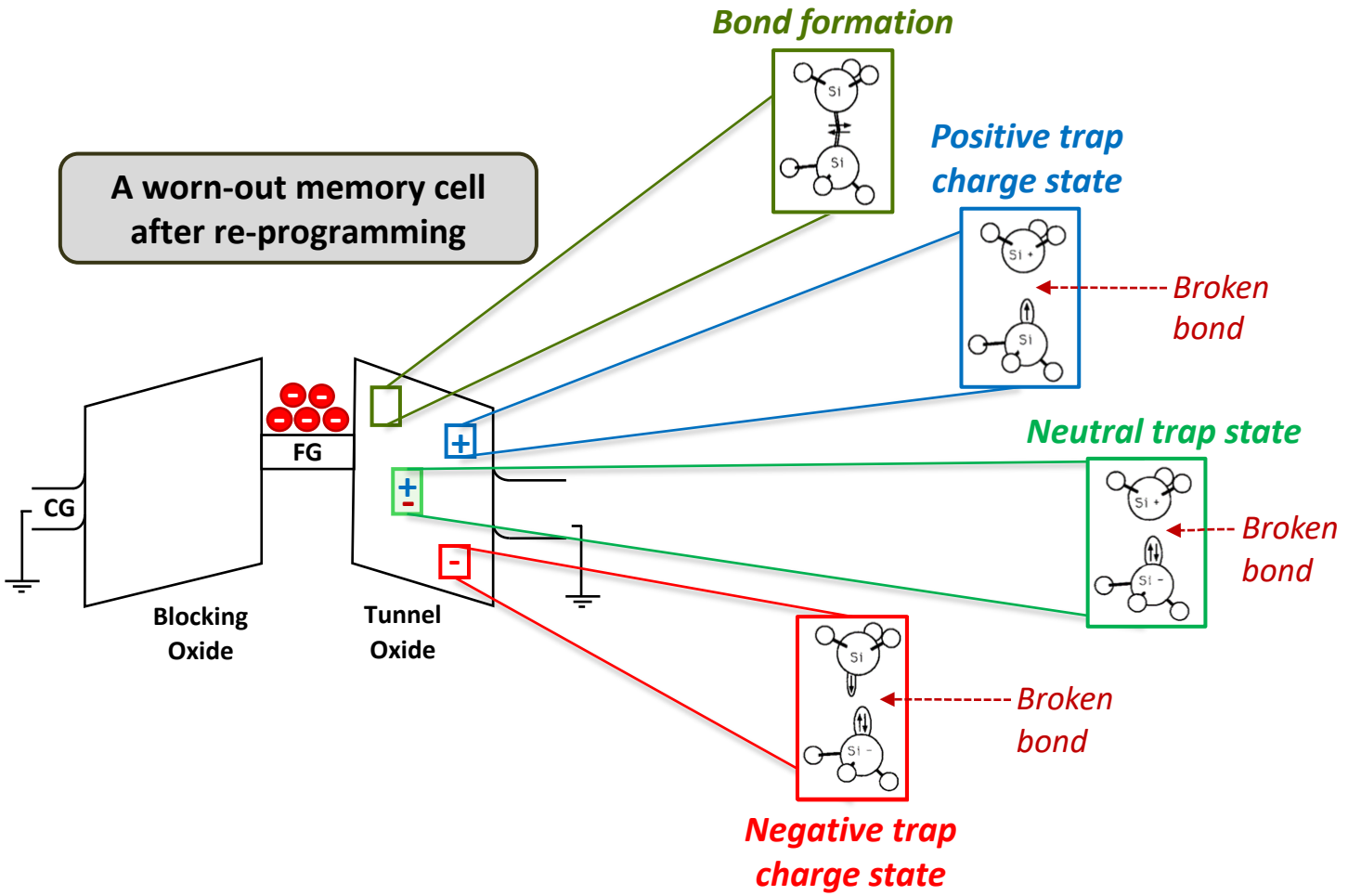


Erase Time



The post-annealed worn-out block can take only ~300 PE cycles extra, which gives ~30% endurance improvement after the first round of thermal annealing. We also observe the improvement in erase time.

Molecular Picture of Oxide Defect



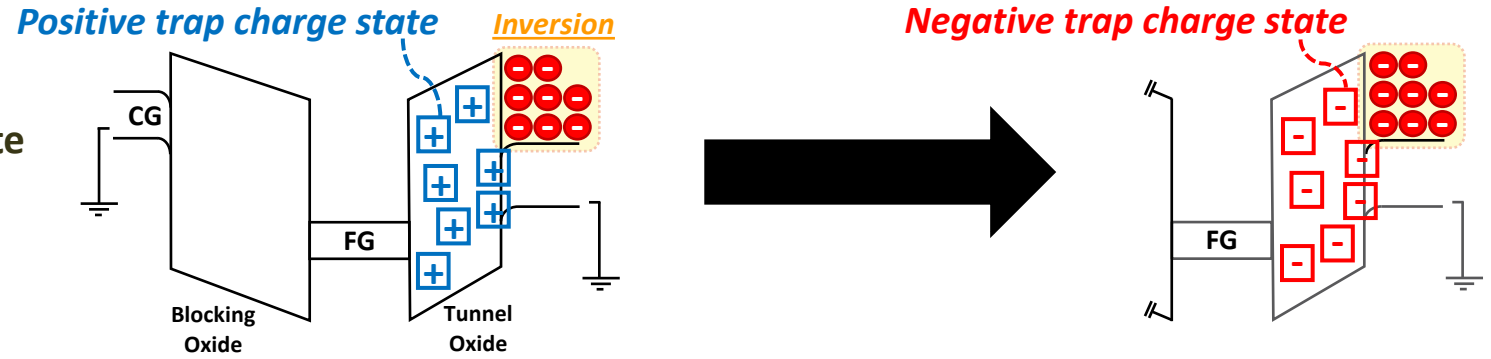
- **Bond formation:** real annealing (Si=Si bonding)
- **Positive trap charge state:** bond is broken, and damage is created
- **Neutral trap state:** positive and negative charges sit next to each other but no bond forming
- **Negative trap charge state:** prevent real annealing or Si=Si bond forming

M. Walters and A. Reisman 1991 J. Electrochem. Soc. 138 2756

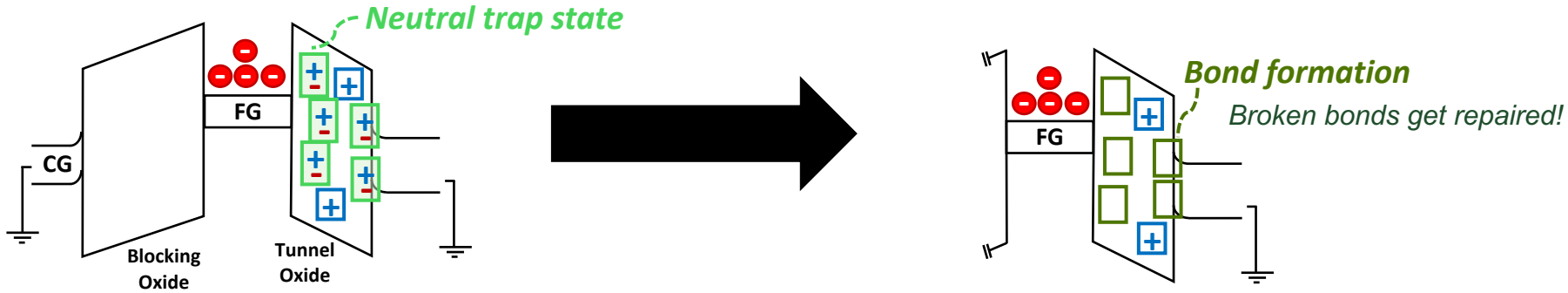
Physics behind Thermal Annealing

Pre-annealing | **Post-annealing**

Case1: Leave in erase state



Case 2: Leave in a programmed state



The positive trap state in the erased memory cell causes electron injections from the channel, preventing the Si=Si bound forming (annealing). The programmed memory cell prevents electron injection from the channel to FG, resulting in true annealing (Si=Si bound).

Conclusion

- This work explores the thermal annealing effects on the endurance of 3D NAND flash memories when reaching the end of their lifetime.
- The experimental evaluation is carried out on commercial 3D FG TLC and MLC NAND flash chips.
- Our experimental results on 3D TLC chips reveal that thermal annealing of the chip in the programmed states offers the highest endurance recovery.
- We find that the post-annealed worn-out block can take only ∼300 PE cycles extra, which gives ∼1,300 PE cycles total before reaching its second lifetime. This leads to ∼30% endurance improvement.
- Moreover, both TLC and MLC chips reveal erase time improvement after thermal annealing.
- Finally, we conclude that the annealing method is applicable to both TLC and MLC 3D NAND flash memory chips.

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Thank you